CLAIMS

What is claimed is:

1. A method comprising:

predicting a first event that allows for lower performance in a processor;

transitioning said processor from a high performance state to a low performance state upon prediction of said first event;

detecting a second event that can utilize greater performance in said processor; and

transitioning said processor from said low performance state to said high performance state upon detection of said second event.

2. The method of claim 1 further comprising detecting a cache miss event.

3. The method of claim 2 wherein said cache miss event causes said processor to fetch data from external memory.

4. The method of claim 3 wherein said detecting a second event comprises monitoring a bus unit for notification of incoming data from a memory fetch.

5. The method of claim 3 wherein said cache miss event causes said processor to stall an instruction pipeline.

6. The method of claim 1 wherein said predicting comprises monitoring processor

signals indicating a cache miss, processor reset, or standby.

7. The method of claim 6 wherein said transitioning from a high performance state to a low performance state comprises powering down idle functional units in said processor.

8. The method of claim 1 wherein said high performance state consumes a greater amount of power than said low performance state.

9. The method of claim 8 wherein said transitioning from a high performance state to a low performance state comprises powering down functional units that are not in use.

10. The method of claim 9 wherein said transitioning from said low performance state to said high performance state comprises powering up functional units that have been powered down.

11. The method of claim 8 wherein said transitioning from a high performance state to a low performance state further comprises slowing down an internal processor core clock signal from a normal operating frequency to a lower frequency.

12. The method of claim 11 wherein said transitioning from said low performance state to said high performance state comprises speeding up said internal processor core clock signal to said normal operating frequency.

13. A processor comprising:

a bus unit to fetch data and interact with an external bus;

a cache memory coupled to bus unit, said cache memory to store data;

an execution unit coupled to said cache memory, said execution to execute instructions; and

a power control circuit coupled to said bus unit, said power control circuit to control when said processor transitions between a high power state and a low power state.

14. The processor of claim 13 further comprising an instruction pipeline coupled to said execution unit, said instruction pipeline to provide said instructions to said execution unit.

15. The processor of claim 14 further comprising a processor core clock generator to provide a clock signal to a plurality of functional units within said processor.

16. The processor of claim 15 wherein said power control unit monitors said execution unit and determines whether to transition said processor from said high power state to said low power state.

17. The processor of claim 16 wherein said power control unit powers down idle functional units within said processor when said processor is transitioned from said high power state to said low power state.

18. The processor of claim 17 wherein said power control unit monitors said bus unit, and to transition said processor from said low power state to said high power state when said bus unit indicates data is incoming on said external bus.

19. The processor of claim 18 wherein said power control unit powers up functional units within said processor that have been powered down when said processor is transitioned from said low power state to said high power state.

20. A system comprising:

a memory coupled to a bus;

a memory controller coupled to said bus;

a processor coupled to said bus, said processor including control logic to determine whether a first event has enabled said processor to be in a low performance state, to transition said processor from a high performance state to said low performance state if said first even has occurred; to detect a second event necessitating said processor to be in said high performance state; and to transition said processor from said low performance state to said high performance state if said second event is detected.

21. The system of claim 20 wherein said first event is a cache miss, wherein said cache miss causes said processor to fetch data from said memory.

22. The system of claim 21 wherein said second event is bus activity due to a memory

read wherein said memory is sending data to said processor.

23. The system of claim 22 wherein said control logic is monitoring an data fetch unit within said processor for cache misses and wherein said control unit is monitoring a bus unit within said processor for bus activity with said memory.

24. The system of claim 20 further comprising a power supply to provide power to said memory, said memory controller, and said processor.

25. The system of claim 24 wherein said power supply can sink current during a transition from a high power state to a low power state, and wherein said power supply can provide current during a transition from said low power state to said high power state.

26. An article comprising a machine readable medium having stored thereon a plurality of instructions which, if executed by a machine, cause the machine to perform a method comprising:

determining whether a first event has enabled a processor to operate in a low performance state;

transitioning said processor from a high performance state to said low performance state if said first event has occurred;

detecting a second event that can necessitates greater performance in said processor; and

transitioning said processor from said low performance state to said high

performance state upon detection of said second event.

27. The article of claim 26 wherein said first event is a cache miss, wherein said cache miss causes said processor to fetch data from memory external to said processor.

28. The article of claim 27 wherein said second event is bus activity resulting from said memory send data to said processor.

29. The article of claim 28 wherein said method further comprises monitoring said processor for cache misses and monitoring a bus for bus activity.

30. The article of claim 26 wherein said machine readable medium is a read only memory (ROM).